Brett Shook

EDA developer specializing in machine learning-driven solutions for digital and mixed signal systems.

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Github
LinkedIn

WORK HISTORY

Self-Employed — *Hardware / Software Development*

Feb. 2024 - Present

Developed an embedded hardware project for a portable wireless security system. Designed and fabricated prototype PCB along with enclosure. Studying RL methods and agentic LLMs in depth.

Motivo — *Principal Software Engineer*

Jan. 2022 - Jan. 2024

Conducted research and development for this startup company regarding machine learning and data mining for the purposes of solving timing closure and optimization of digital circuits. My primary contribution was developing supervised timing estimation models and data mining infrastructure. I also helped develop RL based methods to solve timing closure.

Intel — *Software Engineer*

Apr. 2014 - Jan. 2022

Wrote and maintained software which enables faster more efficient semiconductor design.

Lead developer of **MLParest**, a machine learning based electrical parasitic estimation system. Program used widely across design teams and deployed for many semiconductor technologies. See publications for more info.

Conducting research and development on tools to further automate mixed signal system design with an emphasis on ML to help solve long standing problems in the field.

Extensive experience with custom scripting for Cadence and Synopsys design tools and many other EDA and simulation tools.

Intel — *Graduate Intern*

May 2013 - Sept. 2013

Created a behavioral modeling library in SystemVerilog for high level architectural exploration for mixed signal systems.

Library successfully used in production environments to model high speed serial I/O interfaces such as PCI Express.

SKILLS

Software Architecture Design

Machine Learning

Reinforcement Learning

Digital Timing Closure

Analog and Mixed Signal Simulation & Layout

Multi-Objective Optimization

HDL Behavioral Modeling

Linux General Usage

Docker

EDA SOFTWARE EXPERIENCE

Cadence Virtuoso, Spectre, AMS, QRC Extraction, Liberate-AMS

PrimeTime, Fusion Compiler, Synopsys VCS, VCS-XA, StarRC

Mentor Calibre

OpenROAD, SiliconCompiler

PROGRAMMING LANGUAGES

Python, Java, C++, TypeScript / JS, TCL, SKILL, SystemVerilog, VHDL, Verilog-AMS, SQL

SOFTWARE LIB. / FRAMEWORKS

Pandas, PyTorch, SciKit-Learn

NetworkX, Django

Node JS

University of Arkansas — *Graduate Research Assistant*

Jan. 2011 - Apr. 2014

Conducted research on electronic design automation tools for power electronics.

Lead developer of **PowerSynth**, a power module design synthesis tool. Created the initial software architecture and framework which has been leveraged for many years by successive researchers. This project is highly multidisciplinary involving concepts ranging from multi-objective optimization, finite element analysis, and GUI development (Qt).

https://grapes.uapower.group/
https://e3da.csce.uark.edu/release/PowerSynth/

FlipFire LLC. — *Software Developer*

June 2008 - June 2009

Wrote a distributed video encoding system for this startup company (Java, FFMPEG, Java Server Faces).

Wal-Mart Information Systems Division — *Programming Intern (High School)*

May 2005 - Aug. 2005

Worked with large SQL databases.
Wrote and modified programs for buyer scheduling (C++, Visual Basic)
Gained experience with code repositories and group projects.

EDUCATION

University of Arkansas — *M.S. Electrical Engineering*

Jan. 2011 - Apr. 2014

Thesis: Multi-Chip Power Module Layout Synthesis and Optimization

University of Arkansas — *B.S. Electrical Engineering*

2006 - 2010

Senior Project: Sun tracking solar panel; Embedded electronics design

PUBLICATIONS

"**MLParest: Machine Learning based Parasitic Estimation for Custom Circuit Design**," 2020 57th ACM/IEEE Design Automation Conference (DAC), 2020, pp. 1-6, doi: 10.1109/DAC18072.2020.9218495.

"**Multi-chip power module fast thermal modeling for layout optimization**," Computer-Aided Design & Applications, 9(6), pp. 837-846, 2012.

"**Multi-objective layout optimization for multi-chip power modules considering electrical parasitics and thermal performance**," 2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL), Preprint, 2013.